What is claimed is:

1. A method for hierarchical very large scale integration design comprising:

representing a structure of the hierarchical very large scale integrated design as a graph comprising design objects;

specifying a transformation behavior applied to the design objects; and

processing, top-down, the graph to perform the transformation on the hierarchical very large scale integrated design.

2. The method of claim 1, wherein the processing further comprises searching for an isomorphic structure.

3. The method of claim 1, wherein the graph describes a plurality of scopes.

4. The method of claim 1, wherein the graph is based on a pointset interaction between structures of the hierarchical very large scale integration design.

5. The method of claim 1, wherein the graph is based on symmetry groups between structures of the hierarchical very large scale integration design, wherein the graph represents a circuit substructure.

6. The method of claim 1, wherein an attribute is attached to a design object, the attribute having a user-defined mapping between an attribute transformation and a design object transformation.

7. The method of claim 1, wherein processing, top-down, comprising transferring information from a child graph to a parent graph, wherein a node in the parent graph represent an instance of the child graph.

8. The method of claim 1, wherein processing, top-down, the graph comprises resolving boundary conditions, recursively, by adjusting a parent cell, beginning with a root cell of the graph.

9. The method of claim 8, wherein each cell is represented by a plurality of connected least enclosing orthogonal pointsets.

10. The method of claim 9, further comprising:

determining an interaction between the least enclosing orthogonal pointsets; and

determining a decomposition of the cell according to the interaction.

11. The method of claim 10, wherein processing, top-down, further comprises cloning by expression using a result of the decomposition to produce a cell definition.

12. The method of claim 1, wherein representing the structure of the hierarchical very large scale integration design as the graph comprising design objects further comprises determining a plurality of scopes, wherein each scope comprises an internal node and a leaf node.

13. A method for processing a design graph comprising:

providing a design;

specifying a substructure to be determined within the design as a graph;

deriving design objects from the design;

mapping design objects to nodes of the graph by using a rail and junction decomposition to capture a pointset topology comprising edges;

mapping relationships between design objects to the edges; and

searching the graph for a structure.

14. The method of claim 13, wherein searching comprises searching the graph for an isomorphic substructure known to be an instance of the structure.

15. The method of claim 13, wherein searching comprises searching the graph for a geometric substructure according to a pointset interaction of the graph having mapped design objects and relationships.

16. A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for hierarchical very large scale integration design, the method steps comprising:

representing a structure of the hierarchical very large scale integrated design as a graph comprising design objects;

specifying a transformation behavior applied to the design objects; and

processing, top-down, the graph to perform the transformation on the hierarchical very large scale integrated design.

17. The method of claim 16, wherein the processing further comprises searching for an isomorphic structure.

18. The method of claim 16, wherein the graph describes a plurality of scopes.

19. The method of claim 16, wherein the graph is based on a pointset interaction between structures of the hierarchical very large scale integration design.

20. The method of claim 16, wherein the graph is based on symmetry groups between structures of the hierarchical very large scale integration design, wherein the graph represents a circuit substructure.

21. The method of claim 16, wherein an attribute is attached to a design object, the attribute having a user-defined mapping between an attribute transformation and a design object transformation.

22. The method of claim 16, wherein processing, top-down, comprising transferring information from a child graph to a parent graph, wherein a node in the parent graph represent an instance of the child graph.

23. The method of claim 16, wherein processing, top-down, the graph comprises resolving boundary conditions, recursively, by adjusting a parent cell, beginning with a root cell of the graph.

24. The method of claim 23, wherein each cell is represented by a plurality of connected least enclosing orthogonal pointsets.

25. The method of claim 24, further comprising:

determining an interaction between the least enclosing orthogonal pointsets; and

determining a decomposition of the cell according to the interaction.

26. The method of claim 25, wherein processing, top-down, further comprises cloning by expression using a result of the decomposition to produce a cell definition.

27. The method of claim 16, wherein representing the structure of the hierarchical very large scale integration design as the graph comprising design objects further comprises determining a plurality of scopes, wherein each scope comprises an internal node and a leaf node.